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Design and Analysis of Hybrid 1-Bit Full Adder Circuit and Its Impact on 2-Bit Comparator

Rachana S[1], Roshan Shetty[2], Praveen J[3], Raghavendra Rao A[4]

M.Tech Student, Dept. of ECE, Alva's Institute of Engg & Technology, Mijar, Moodbidri, Karnataka, India[1]

Assistant Professor, Dept. of ECE, Alva's Institute of Engg & Technology, Mijar, Moodbidri, Karnataka, India [2, 3,4]

Abstract: Full adder structures are used as a basic and essential blocks to build any VLSI and embedded applications. So it demands the researchers to design low power and low speed full adder circuits to improve efficiency of the design. This project deals with a design of 1-bit hybrid adder circuit by incorporating CMOS and transmission gate logic. Simulations are done using Tanner EDA Tools v.13.0. Parameters of designs like delay and power are measured and power delay product are tabulated and are compared with the prior literatures that includes CMOS logic, CPL, TGA and TFA. Power consumption is found to be decreased and delay also reduced greatly. Also all the adders which are designed from previous literatures and proposed full adder circuits are placed in a 2-bit comparator individually and performance of 2-bit comparator will be analyzed. The comparator designed with proposed full adder circuit shows less power and reduced delay, hence better power delay product compared to others.

Keywords: Comparator, hybrid design, low power, CMOS (Complementary Metal Oxide Semiconductor), high speed, power delay product, Tanner tool.

I. INTRODUCTION

Portable devices such as mobile phones, notebooks, laptops etc. use batteries for their operations. Usages of these devices are increasing these days. This demands for less power and reduced delay VLSI designs. All the above mentioned applications require full adder circuits for their implementations. Full adder circuits are the key domain for the researchers to focus on, over the years. Also basic operation in arithmetic is addition and it acts as a core for other operations like subtraction, multiplication, division etc. Many VLSI systems requires adders for their implementation. So in a modern electronics, designing of accurate and fast full adder circuits that leads to long lasting battery operated designs is the major element. Thus the full adder design concentrates on two main factors, i.e., speed escalation and power consumption devaluation [5].
In very large integrated circuits (VLSI), challenge is to design a circuit that can operate with lesser supply voltages. By reducing the supply voltage, circuit may not work according to the desire and it may affect the overall design implementation. Here the adders are designed with less supply voltages. Performance analysis is measured by taking various considerations like power dissipation, total propagation delay and transistor count. Hence the power delay product (PDP) for the circuit [1] also calculated. Over the years, adders are designed by using different logic techniques. Each design is having both advantages and disadvantages. Under different loads, the circuit design should process good drivability balanced output in order to avoid glitches. Major factors associated with power dissipation are transistors size, number, capacitance in a node, complexity of a wire, switching activity. The average power will be equal to sum short circuit, dynamic and static powers. During switching activity, each gate will consume some amount of energy and it is represented as PDP. It's a measure of efficiency in an adder.

PDP = power * delay

A. BASICS OF FULL ADDER

Fig.1 gives the basic block level representation of full adder. This circuit will have three inputs taken as A, B, and Cin. Outputs of the circuit will be taken as SUM and Cout.

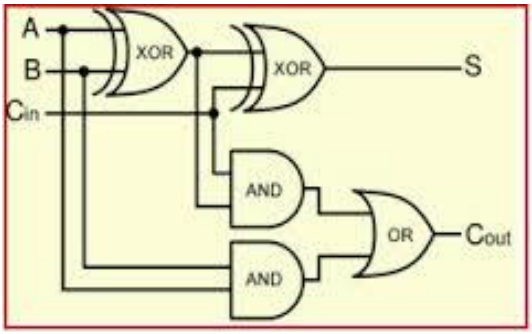

Fig.1 Basic block diagram of full adder circuit

The Sum and Cout are taken as
Sum = A exor B exor Cin
Cout = AB + BCin + ACin
If, A=B, then Cout=B; else Cout=Cin.

II. DESIGN IMPLEMENTATION

In this section, conventional approaches of a full adder circuits like CCMOS, CPL, TGA, TFA and proposed architecture of a full adder circuits are discussed**.**

A. Classical Complementary Metal-Oxide- Semiconductor (CCMOS) Full Adder

Classical designs which are used to design the full adder circuits make use of single logic technique to implement

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the entire design. CMOS adder structure is an example for this kind of design. The CMOS adder contains 28T. This structure resembles normal CMOS where, PMOS transistors (14T) are placed in pull-up network and NMOS transistors (14T) are placed in pull-down network. The schematic diagram for CCMOS adder is available in Fig.2.

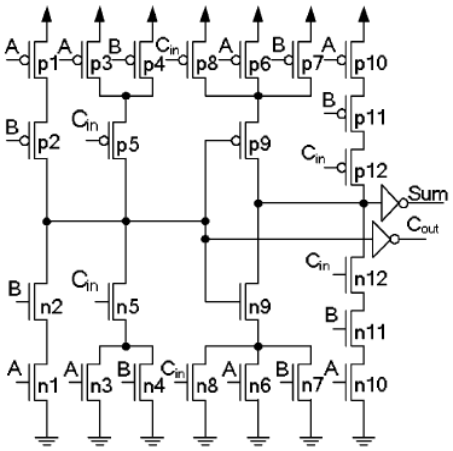

Fig.2 CCMOS (28T)

1. Advantages:

The main advantage of CCMOS full adder is, it has a high noise margins. Hence it will operate under lower voltages reliably. It contains a complementary transistor pairs, so the layout of this design also simplified (layout regularity). This adder has robustness against transistor sizing and voltage scaling [9].

2. Disadvantages:

In this design, each input is connected to either PMOS or NMOS gates, so it results in large input capacitance and also results in degradation of speed. In the output stage, it has transistors in series that forms a weak driver. Because of this reason, additional buffers are placed at the final stage. It provides necessary power to drive the cells that are cascaded and hence results in large silicon area. This full adder structure contains more number of PMOS devices. It is a main disadvantage because in order to get a desired performance, sizing has to be carried out for PMOS devices. Also, PMOS devices exhibit lower mobility than that of NMOS. It makes use of CMOS devices in order to generate sum which results in additional unwanted delay. Sub threshold leakage will be more, since there are many leakage paths.

B. Complementary Pass-Transistor Logic (CPL)

Adder design using this technique contains 32 transistors in a dual rail structure. Main difference between CPL and CCMOS full adders is that, in a pass transistor logic circuit, input signals connects to the source side instead connecting them to power lines. Also, speed of operation is better in CPL than CCMOS. Schematic diagram of CPL adder is given in Fig.3.

1. Advantages:

The main advantage here is, single pass transistor is required in order to design any logic. It results in less transistor count and less input loading. It has lower input impedance and output voltage will be less. It is capable of swing restoration. Since it has better output driving capability and faster differential stages, it makes very efficient implementation of complex gates. Most prime feature of CPL is its small stack height that results in less consumption of power.

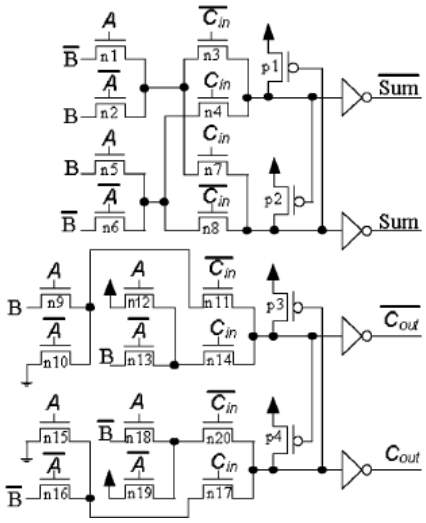

Fig.3 CPL (32T)

Swing Restored Pas- transistor Logic (SRPL) is designed using CPL. In this SRPL style, latch structure is formed by cross coupled output inverters. This results in swing restoration along with output buffering. In order to reduce the power in CPL circuits, SRPL and LCPL circuits are used. DC power is reduced to attain full swing operation by using complementary transistors in Double Pass-Transistor Logic. Hence the restoration circuitry is eliminated.

2. Disadvantages:

Pass transistor logic suffer from voltage drop problem. i.e., when “1” is given as a input to the NMOS, output will be weaker logic “1” because NMOS is a strong passer of “0”. In a same way, when “0” is given as a input to PMOS, output will be weaker logic “0” as PMOS is a strong passer of “1”. There are more number of intermediate nodes, more number of transistors and overloading of inputs which results in higher switching activity that in turn consumes more power. CPL does not suit for applications with lesser power since it has a high degree of wiring complexity, more delay. It gives complementary outputs as it takes complementary inputs.

CPL cell layout is not straightforward compare to CMOS because of irregularity in transistor arrangements. CPL suffers because of static power loss at the output inverter gates due to low swing. In this adder architecture, inputs and outputs both will be in true and complement form. It results in larger short circuit currents and wiring overhead is more.

C. TRANSMISSION GATE ADDER (TGA)

Special case of pass transistor logic is transmission gate logic. This adder structure contains 20 transistors which consist of complementary NMOS (10T) and PMOS (10T) transistor properties. It is designed by connecting NMOS

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transistor in parallel with PMOS transistor that is controlled by control signals in a complementary form. When NMOS and PMOS transistors turn on simultaneously, then transmission gate will provides a path for input logic "1" or "0". Hence there will be no voltage drop in the circuit. Schematic diagram of TGA is provided in Fig.4.

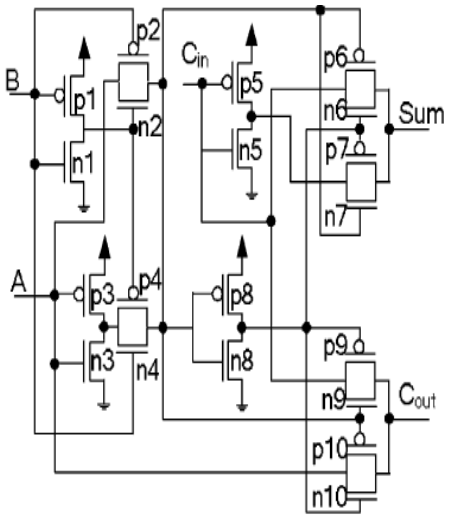

Fig.4 TGA (20T)

1. Advantages:
The circuit is very simple when compared to other conventional adders, hence results in faster operations. Power consumption will be similar to that of CMOS, but it performs faster. Here transistor counts are less resulting in lesser delay compared to CPL and CCMOS full adders. This logic style is well suited for designing XOR or XNOR gates. Performance of the circuit degrades when it is connected in cascade.

2. Disadvantages:
Twice the number of transistors is required to design the circuit that can be implemented by pass transistor logic. It has a low driving capability. Followed by two transmission gates, circuit contains two inverters, together they acts as 8-T XOR.
Number of internal nodes will be more in this architecture. Hence parasitic capacitance will be more. It gives a poor performance in a arithmetic circuits due to additional buffers at output stage, increasing the power dissipation.

D. TRANSMISSION FUNCTION ADDER (TFA)
This adder structure is designed using transmission function theory. This adder uses 16T for its operation which includes transmission gates, pass transistors and low power XNOR and XOR gates. Schematic diagram of TFA is presented in Fig.5.

1. Advantages:
Full adder designed with this logic consumes less power and offers higher speed reducing the delay compare to other conventional adders. This logic proves to be a good choice to design XOR and XNOR gates. It gives same delay for both sum and Cout. As the transistor count required to implement full adder is less, it results in less power and less silicon area. In terms of power and leakage, this adder gives better performance.

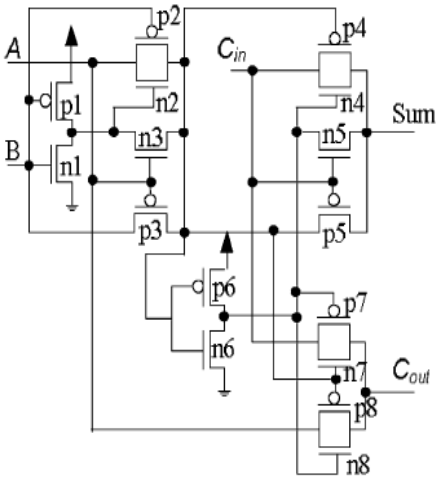

Fig.5 TFA (16T)

2. Disadvantages:
Full swing outputs are not obtained by XOR and XNOR modules, so the transistors that are connected to this module turns on or off slowly. Adder designed with transmission function logic suffers from lack of driving capability. There is a significant degradation of performance when it is cascaded.

E. PROPOSED HYBRID 1-BIT FULL ADDER CIRCUIT
Proposed adder architecture uses both transmission gate logic and CMOS logic for its implementation. Here, full adder is represented by a 3 blocks or modules. For the generation of output sum signal (SUM), we make use of XNOR modules and they are represented by module 1 and module 2. Generation of carry signal (Cout) is through module 3. Block representation of proposed full adder is given in Fig.6.

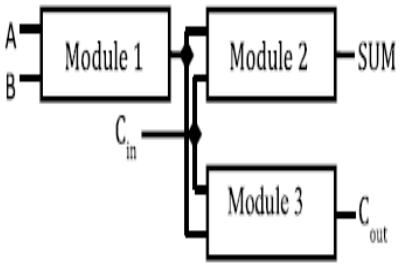

Fig.6 Block diagram of proposed full adder

Each module is independently designed so that the entire circuit will be optimized with respect to delay, power and area. The modules are discussed below. The internal architecture of module 1 and 2 are represented in Fig.7 which is used for generation of sum. Module 3 is represented in Fig.8.

1. MODIFIED XNOR MODULE
XNOR module consumes more power in the proposed adder design. Power can be minimized to best possible extent by optimizing the XNOR module. It also avoids the

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possibility of voltage degradation. Fig.7 represents Modified XNOR circuit.

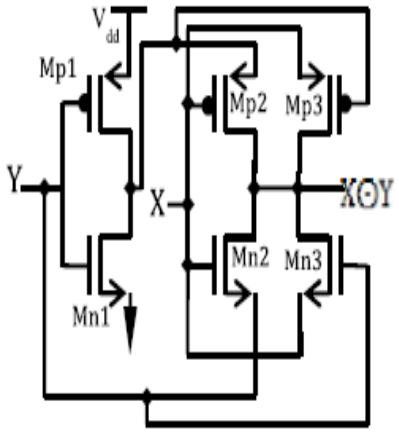

Fig.7 Schematic diagram of XNOR module

Here there is a significant reduction in power as it makes use of a weak inverter (transistors having small channel width). In a Fig, Mp1 and Mn1 form a weak inverter. Mp3 and Mn3 are referred as level restoring transistors which results in fall swing of output signals. The XOR/XNOR circuits that are designed in prior literatures uses 6 transistors to give better output swing. Here also XNOR module consists of 6 transistors but, the arrangement of transistors are different. It is arranged in such a manner that, it gives lower power and higher speed compared to other literatures.

2. CARRY GENERATION MODULE

The schematic of this module is given in Fig.8. The transistors Mp7, Mn7, Mp8 and Mn8 are implemented in order to achieve the output carry signal. Here input carry signal (Cin) passes or propagates through only one transmission gate, i.e., Mn7 and Mp7. Hence it reduces path required for carry propagation. Large channel width transistors are used for transmission gates. Here Mn7, Mp7, Mn8 and Mp8 form the transmission gates. Hence it results in reducing the delay for some extent.

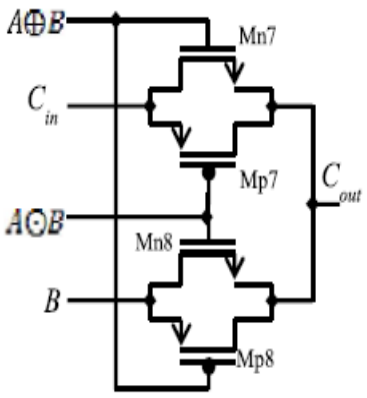

Fig.8 Schematic diagram of carry generation module

3. OPERATION OF PROPOSED FULL ADDER

Detailed circuit for proposed adder is given in Fig.9. Implementation of sum output is through XNOR modules. The generation of input signal B is from a inverter with transistors Mp1 and Mn1. This in turn used in the design of controlled inverter comprising of Mp2 and Mn2. The controlled inverter output will be XNOR of A and B. this operation has a problem with degradation of voltage. This can be eliminated by use of 2 pass transistors namely MP3 and Mn3.

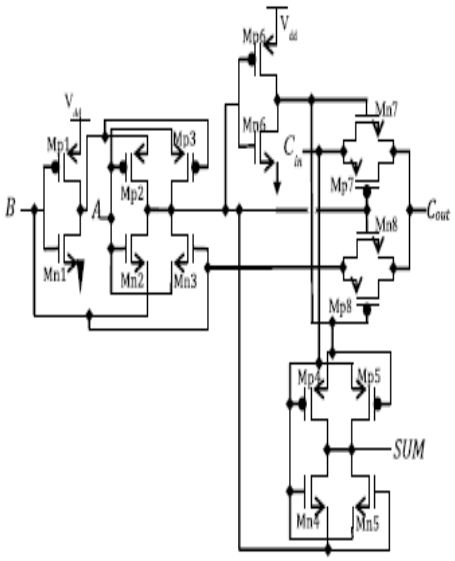

Fig.9 Detail circuit diagram of proposed full adder

In a same way, NMOS transistors Mn4, Mn5, Mn6 and also PMOS transistors Mp4, Mp5, Mp6 are used as a second module of XNOR gates which results in the output sum signal. The output carry is obtained through transistors Mn7, Mp7, Mn8 and Mp8. For the full adder circuit, carry out is analyzed as follows. If A is equal to B, then Cout will be equal to B. otherwise, Cout will be equal to Cin.

F. DESIGN OVERVIEW: 2-BIT COMPARATOR

2-bit comparator circuit is taken here as a application circuit. Full adder based comparator circuit is designed which is used in a block of ALU.

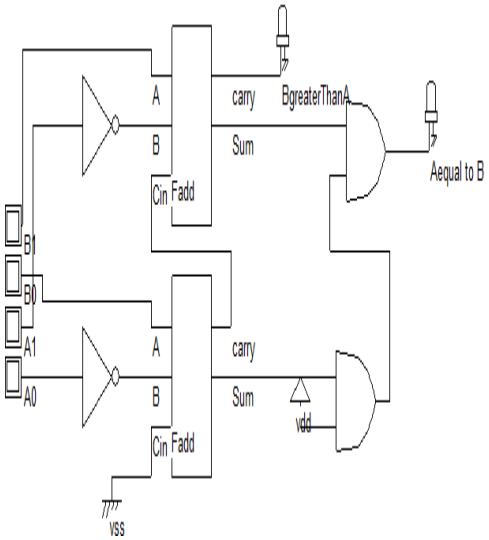

Fig.10 Comparator using full adder

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In order to compare two numbers in digital systems, magnitude comparators are used. Main objective here is to optimize delay, power and silicon area. Comparators are designed by using conventional full adder circuits and also by using proposed hybrid full adder circuit. Its performance is measured based on delay, power and power delay product. 2-bit comparator circuit that uses full adders for its operation is as shown in Fig.10.

III. SIMULATION RESULTS

Different types of full adders are designed using Tanner EDA Tools 13.0 Licensed Version in this project. It includes schematic designs and analysis of conventional full adders and proposed full adder. Different analysis on both conventional and proposed adder designs is carried out. They include power analysis, delay analysis and calculating PDP. VLSI design involves low voltage implementation and low power implementation in its design in order to get optimized performance. Here the circuits are designed using 1V supply as VDD that results in minimum propagation delay and lower power consumption.

A. The CCMOS Full Adder – Full Adder 1

1. Schematic Diagram

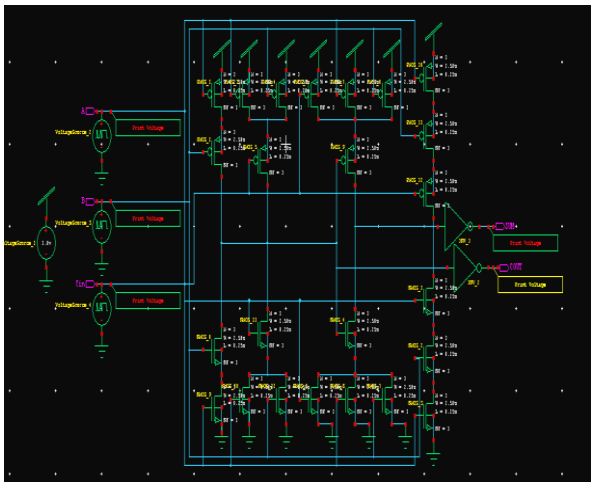

Fig.11 Schematic Representation of Full Adder 1

2. Output Waveforms

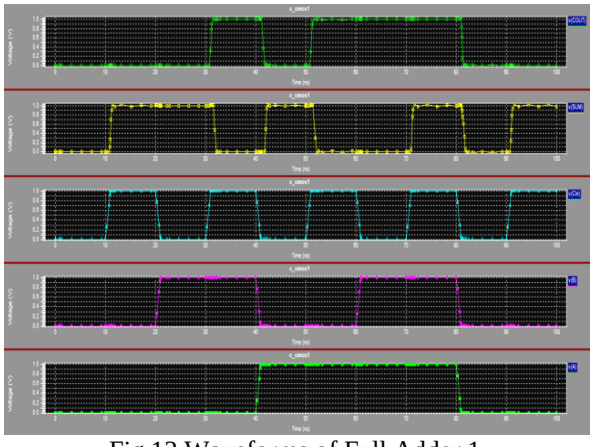

Fig.12 Waveforms of Full Adder 1

3. Power and delay Analysis

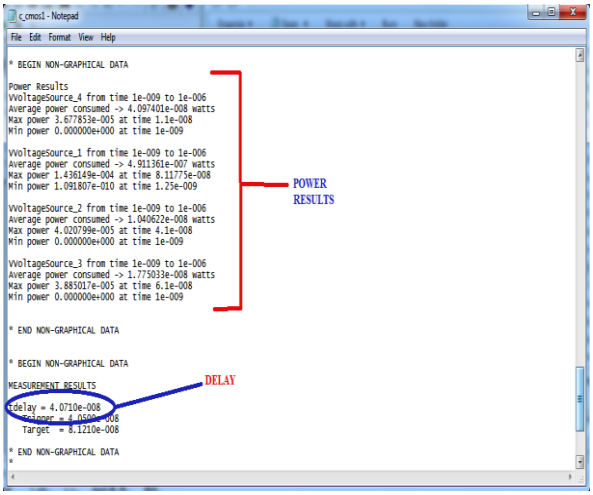

Fig.13 Power and Delay results of Full Adder 1

4. Comparator design by incorporating CCMOS Full Adder (Full Adder 1) – Comparator 1

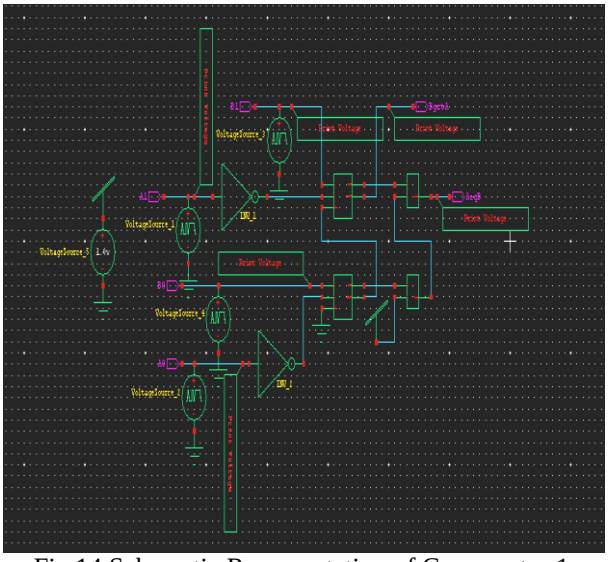

Fig.14 Schematic Representation of Comparator 1

5. Output Waveforms

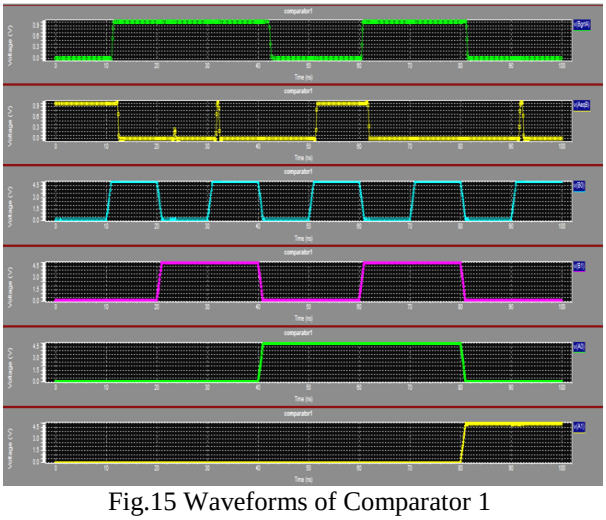

Fig.15 Waveforms of Comparator 1

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6. Power and delay analysis

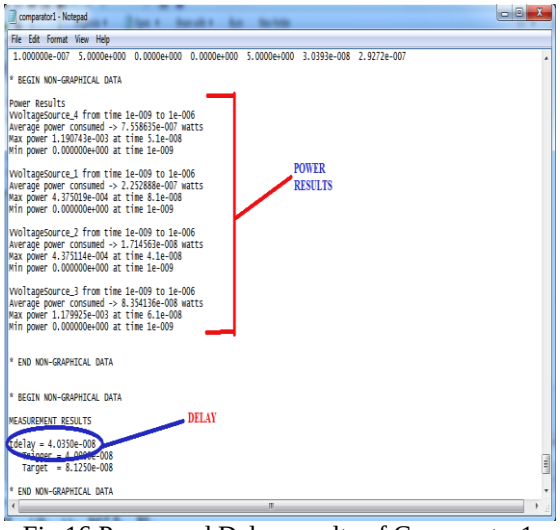

Fig.16 Power and Delay results of Comparator1

B. The Complementary Pass Transistor Logic Full Adder – Full Adder 2
1. Schematic Diagram

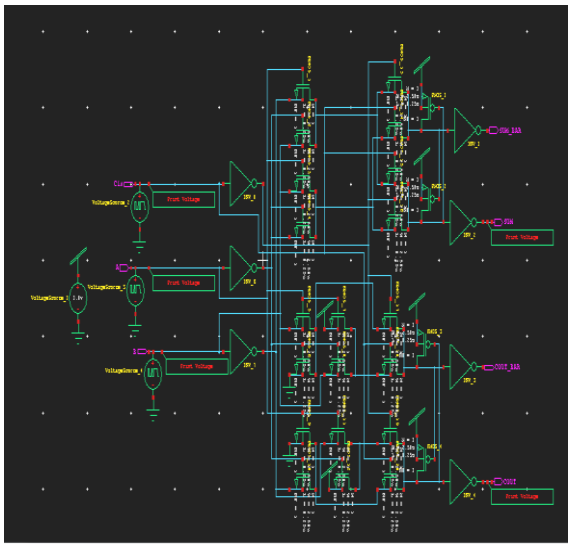

Fig.17 Schematic Representation of Full Adder 2

C. Transmission Gate Adder - Full adder 3
1. Schematic Diagram

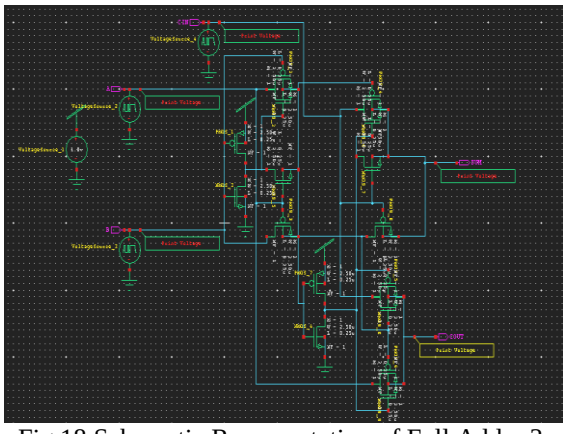

Fig.18 Schematic Representation of Full Adder 3

D . Transmission Function Full adder – Full adder 4
1. Schematic Diagram

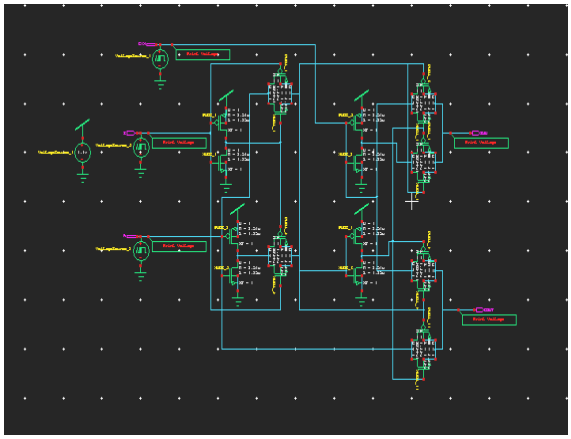

Fig.19 Schematic Representation of Full Adder 4

E. Hybrid 1-bit Full Adder - Full Adder 5
1. Schematic Diagram

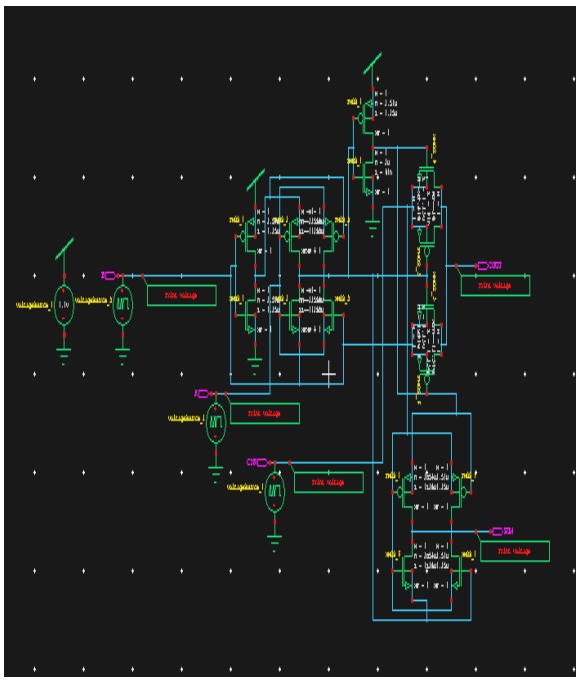

Fig.20 Schematic Representation of Full Adder 5

F. COMPARISON RESULTS
A. Comparison between Power, Delay and PDP of all Full Adders

Table 1: Comparison between Power, Delay, PDP and Transistor Count of all full adders

Sl. No	Full Adders	Power (mW)	Delay (mS)	PDP (uJ)	Transistor Count
1.	**CCMOS**	6.79	1.36	9.23	28
2.	**CPL**	7.95	1.38	10.97	32
3.	**TGA**	6.61	1.34	8.85	20
4.	**TFA**	7.055	0.68	4.79	16
5.	**PROPOSED**	6.34	0.33	2.09	16

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B. Comparison between Power, Delay and PDP of all Comparators

Table 2: Comparison between Power, Delay, PDP and Transistor Count of all comparators

Sl. No	Comparators	Power (mW)	Delay (mS)	PDP (uJ)
1	**CCMOS**	16.669	1.353	22.553
2	**CPL**	13.571	1.342	18.212
3	**TGA**	10.559	1.343	14.180
4	**TFA**	10.698	0.724	7.745
5	**PROPOSED**	7.458	1.152	1.336

IV. CONCLUSION AND FUTURE WORK

The main intension in this project is to minimize the power consumption and to reduce the propagation delay, so that the performance and speed of the circuit will be improved. Here both conventional and proposed full adders are designed using Tanner EDA licensed version 13.0., in 90nm technology at 1V. The designed schematic and the results of simulation shows that the proposed adder i.e., Hybrid 1-bit full adder circuit gives very less power consumption and also greatly reduces the propagation delay, hence PDP will be less. This is due to coupling of weaker CMOS inverters to the strong transmission gates. The results are compared with conventional full adders like CCMOS, CPL, TGA, and TFA.

2-bit comparator is designed by incorporating all conventional full adders and proposed adder. The impact of proposed hybrid 1-bit full adder on comparator 5 results in improved PDP, reduced delay and minimum power consumption. Hence the overall circuit performance is improved.

The future work of this project includes the following

- Designing area efficient full adder.
- Optimizing the design of comparator.
- Different analysis to be carried out on a full adder and comparator circuits.

REFERENCES

[1] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SiPS) Taipei, Taiwan, Oct. 1999, pp. 713–722.
[2] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS full-adders for energy-efficient arithmetic applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 718–721, Apr. 2011.
[3] Vandana Choudhary Rajesh Mehra, " 2- Bit Comparator Using Different Logic Style of Full Adder," International Journal of Soft Computing and Engineering (IJSCE), Vol.3, Issue 2, May 2013.
[4] M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Golmakani, "Design of new full adder cell using hybrid-CMOS logic style," in Proc. 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS), Dec. 2011, pp. 451–454.
[5] S. Wairya, G. Singh, R. K. Nagaria, and S. Tiwari, "Design analysis of XOR (4T) based low voltage CMOS full adder circuit," in Proc. IEEE Nirma Univ. Int. Conf. Eng. (NUiCONE), Dec. 2011, pp. 1–7.
[6] P. Prashanth and P. Swamy, "Architecture of adders based on speed, area and power dissipation," in Proc. World Congr. Inf. Commun. Technol. (WICT), Dec. 2011, pp. 240–244.
[7] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEE Proc.-Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.
[8] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-power high-speed hybrid CMOS full adder for embedded system," in Proc.IEEE Conf. Design Diagnostics Electron. Circuits Syst., vol. 13.Apr. 2007, pp. 1–4.
[9] S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.
[10] C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.
[11] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in Proc. Int. Symp. Circuits Syst., May 2003, pp. 317–320.
[12] S. Goel, M. Elgamel, and M. A. Bayoumi, "Novel design methodology for high-performance XOR-XNOR circuit design," in Proc. 16th Symp. Integr. Circuits Syst. Design (SBCCI), Sep. 2003, pp. 71–76.
[13] Hassoune, D. Flandre, I. O'Connor, and J. Legat, "ULPFA: A new efficient design of a power-aware full adder," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 2066–2074, Aug. 2010.
[14] M. Alioto, G. Di Cataldo, and G. Palumbo, "Mixed full adder topologies for high-performance low-power arithmetic circuits," Microelectron. J., vol. 38, no. 1, pp. 130–139, Jan. 2007.
[15] Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar and Anup Dandapat, "Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit," IEEE Trans. on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 10, Oct 2015.